1. A process for forming an adjustable capacitor, comprising:

providing a silicon wafer having a topmost layer on which are contact pads connected to a circuit contained in said wafer;

depositing a base dielectric layer on said topmost layer, including said contact pads;

depositing an etch stop layer on said base dielectric layer;

depositing a support dielectric layer on said etch stop layer;

etching a via hole through said support dielectric layer, said etch stop layer, and said base dielectric layer, thereby exposing said contact pad;

depositing a barrier layer in said via hole, then overfilling said via hole with tungsten and then planarizing so as to remove all tungsten not inside said via;

etching three trenches that extend through said support dielectric layer as far as said etch stop layer;

depositing a first layer of metal on said support dielectric layer, including inside said trenches, and then patterning said first metal layer to form a common capacitor electrode that contacts said tungsten-filled via hole;

depositing a layer of high dielectric constant material on said common capacitor electrode and then patterning said high dielectric constant layer whereby it fully overlaps said common capacitor electrode;

depositing a second layer of metal on said high dielectric constant layer and then patterning said second metal layer to form four unconnected top electrodes, all of whom are overlapped by said common electrode, said top electrodes having, relative to one

another, areas in the ratio 5:2:1:1;

depositing a top dielectric layer on said top electrodes and said high dielectric constant layer;

etching four via holes through said top dielectric layer whereby a contact area is exposed for each of said top electrodes;

depositing a barrier layer in said via holes, then overfilling said via holes with tungsten and then planarizing so as to remove all tungsten not inside said via holes; and

then depositing and patterning a third metal layer so as to provide permanent connections between said top electrodes, thereby giving said adjustable capacitor a specific capacitance value.

2. The process described in claim 1 wherein said base dielectric layer is selected from the group consisting of silicon oxide, TEOS, black diamond, and all dielectrics having a dielectric constant less than about 5 and said base dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms .

3. The process described in claim 1 wherein said etch stop layer is selected from the group consisting of silicon nitride and silicon carbide and is deposited to a thickness between about 20 and 500 microns.

4. The process described in claim 1 wherein said support dielectric layer is selected

from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said support dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

5. The process described in claim 1 wherein said metal layers are selected from the group consisting of Al, Ti, TiN, and all metals whose resistivity is less than about 5 microhm-cm, and are deposited to a thickness between about 200 and 5,000 Angstroms.

6. The process described in claim 1 wherein said layer of high dielectric constant material is selected from the group consisting of silicon nitride, tantalum oxide, aluminum oxide, and hafnium oxide and is deposited to a thickness between about 20 and 500 Angstroms.

7. The process described in claim 1 wherein each trench has a width between about 0.1 and 0.8 microns and said trenches are separated from one another by between about 0.1 and 0.8 microns.

8. A process for forming a field programmable capacitor, comprising:

providing a silicon wafer having a topmost layer on which are contact pads connected to a circuit contained in said wafer;

depositing a base dielectric layer on said topmost layer, including said contact pads;

depositing an etch stop layer on said base dielectric layer;

depositing a support dielectric layer on said etch stop layer;

etching a via hole through said support dielectric layer, said etch stop layer, and said base dielectric layer, thereby exposing said contact pad;

depositing a barrier layer in said via hole, then overfilling said via hole with tungsten and then planarizing so as to remove all tungsten not inside said via;

etching three trenches that extend through said support dielectric layer as far as said etch stop layer;

depositing a first layer of metal on said support dielectric layer, including inside said trenches, and then patterning said first metal layer to form a common capacitor electrode that contacts said tungsten-filled via hole;

depositing a layer of high dielectric constant material on said common capacitor electrode and then patterning said high dielectric constant layer whereby it fully overlaps said common capacitor electrode;

depositing a second layer of metal on said high dielectric constant layer and then patterning said second metal layer to form four unconnected top electrodes, all of whom are overlapped by said common electrode, said top electrodes having, relative to one another, areas in the ratio 5:2:1:1;

depositing a top dielectric layer on said top electrodes and said high dielectric constant layer;

etching four via holes through said top dielectric layer whereby a contact area is

exposed for each of said top electrodes;

depositing a barrier layer in said via holes, then overfilling said via holes with tungsten and then planarizing so as to remove all tungsten not inside said via holes; and

then depositing and patterning a third metal layer to form a contact wire for each of said filled via holes; and

connecting said contacting wires to each other through field programmable devices, thereby forming said field programmable capacitor.

9. The process described in claim 8 wherein said field programmable devices are selected from the group consisting of fusible links, anti-fuses, pass transistors, resistors, and capacitors.

10. The process described in claim 8 wherein said base dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said base dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

11. The process described in claim 8 wherein said etch stop layer is selected from the group consisting of silicon nitride and silicon carbide and is deposited to a thickness between about 20 and 500 microns.

12. The process described in claim 8 wherein said support dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said support dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

13. The process described in claim 8 wherein said metal layers are selected from the group consisting of Al, Ti, TiN, and all metals whose resistivity is less than about 5 microhm-cm, and are deposited to a thickness between about 200 and 5,000 Angstroms.

14. The process described in claim 8 wherein said layer of high dielectric constant material is selected from the group consisting of silicon nitride, tantalum oxide, aluminum oxide, and hafnium oxide and is deposited to a thickness between about 20 and 500 Angstroms.

15. The process described in claim 8 wherein each trench has a width between about 0.1 and 0.8 microns and said trenches are separated from one another by between about 0.1 and 0.8 microns.

16. An adjustable capacitor, comprising:

a silicon wafer having a topmost layer on which are contact pads connected to a circuit contained in said wafer;

a base dielectric layer on said topmost layer and said contact pads;

an etch stop layer on said base dielectric layer;

a support dielectric layer on said etch stop layer;

a tungsten via, extending through said support dielectric layer, said etch stop layer, and said base dielectric layer, and contacting said contact pad;

three trenches that extend through said support dielectric layer as far as said etch stop layer;

a common capacitor electrode on said support dielectric layer, including inside said trenches, that contacts said tungsten via;

on said common capacitor electrode, a layer of high dielectric constant materia that fully overlaps said common capacitor electrode;

on said high dielectric constant layer, four unconnected top electrodes, all of whom are overlapped by said common electrode, said top electrodes having, relative to one another, areas in the ratio 5:2:1:1;

a top dielectric layer on said top electrodes and said high dielectric constant layer;

four tungsten vias, extending through said top dielectric layer, that contact each top electrode, one such via per electrode; and

on said top dielectric layer, permanent electrical connections between said top electrodes, whereby said adjustable capacitor has a specific capacitance value.

17. The capacitor described in claim 16 wherein said base dielectric layer is selected

from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said base dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

18. The capacitor described in claim 16 wherein said etch stop layer is selected from the group consisting of silicon nitride and silicon carbide and is deposited to a thickness between about 20 and 500 microns.

19. The capacitor described in claim 16 wherein said support dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said support dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

20. The capacitor described in claim 16 wherein said common capacitor electrode and said top electrodes are a metal selected from the group consisting of Al, AlCu, Cu, Ti, TiN, and Ta and have a thickness between about 200 and 5,000 Angstroms.

21. The capacitor described in claim 16 wherein said layer of high dielectric constant material is selected from the group consisting of silicon nitride, tantalum oxide, aluminum oxide, and hafnium oxide and is deposited to a thickness between about 20 and 500 Angstroms.

22. The capacitor described in claim 16 wherein each trench has a width between about 0.1 and 0.8 microns and said trenches are separated from one another by between about 0.1 and 0.8 microns.

23. A field programmable capacitor, comprising:

a silicon wafer having a topmost layer on which are contact pads connected to a circuit contained in said wafer;

a base dielectric layer on said topmost layer and said contact pads;

an etch stop layer on said base dielectric layer;

a support dielectric layer on said etch stop layer;

a tungsten via, extending through said support dielectric layer, said etch stop layer, and said base dielectric layer, and contacting said contact pad;

three trenches that extend through said support dielectric layer as far as said etch stop layer;

a common capacitor electrode on said support dielectric layer, including inside said trenches, that contacts said tungsten via;

on said common capacitor electrode, a layer of high dielectric constant materia that fully overlaps said common capacitor electrode;

on said high dielectric constant layer, four unconnected top electrodes, all of whom are overlapped by said common electrode, said top electrodes having, relative to one another, areas in the ratio 5:2:1:1;

a top dielectric layer on said top electrodes and said high dielectric constant layer;

four tungsten vias, extending through said top dielectric layer, that contact each top electrode, one such via per electrode; and

on said top dielectric layer, a metallic contact wire for each of said filled via holes, said contact wires being connectable to each other through field programmable devices.

24. The capacitor described in claim 23 wherein said field programmable devices are selected from the group consisting of fusible links, anti-fuses, and pass transistors.

25. The capacitor described in claim 23 wherein said base dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said base dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

26. The capacitor described in claim 23 wherein said etch stop layer is selected from the group consisting of silicon nitride and silicon carbide and is deposited to a thickness between about 20 and 500 microns.

27. The capacitor described in claim 23 wherein said support dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said support dielectric layer is deposited to a

thickness between about 200 and 5,000 Angstroms.

28. The capacitor described in claim 23 wherein said common capacitor electrode and said top electrodes are a metal selected from the group consisting of Al, AlCu, Cu, Ti, TiN, and Ta and have a thickness between about 200 and 5,000 Angstroms.

29. The capacitor described in claim 23 wherein said layer of high dielectric constant material is selected from the group consisting of silicon nitride, tantalum oxide, aluminum oxide, and hafnium oxide and is deposited to a thickness between about 20 and 500 Angstroms.

30. The capacitor described in claim 23 wherein each trench has a width between about 0.1 and 0.8 microns and said trenches are separated from one another by between about 0.1 and 0.8 microns.